

TET2200-12-086xA Series

AC-DC Front-End Power Supply

The TET2200-12-086 Series is a 2200 Watt AC-DC power-factor-corrected (PFC) and DC/DC power supply that converts standard AC mains power or high voltage DC bus voltages into a main output of 12 VDC for powering intermediate bus architectures (IBA) in high performance and reliability servers, routers, and network switches.

The TET2200-12-086 Series meets international safety standards and displays the CE-Mark for the European Low Voltage Directive (LVD).



Key Features & Benefits

- Best-in-class, 80 PLUS certified “Titanium” efficiency
- Wide input voltage range: 180 - 264 VAC / 2200 W, 90 - 180 VAC /1200 W
- AC input with power factor correction
- Always-on 42 W standby output (12 V / 3.5 A)
- Hot-plug capability
- Parallel operation with active current sharing through analog bus
- Full digital controls for improved performance
- High density design: 53.1 W/in³
- Small form factor: 86.3 x 39.3 x 196.5 mm (3.4 x 1.5 x 7.7 in)
- Up to 400 kHz
- I2C communication interface with Power Management Bus protocol for monitoring, control, and firmware update via bootloader
- Overtemperature, output overvoltage and overcurrent protection
- RoHS Compliant
- Status LED with fault signaling

Applications

- High Performance Servers
- Routers
- Switches



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1. ORDERING INFORMATION

| | | | | | | | | |
|-----------------------|--------------------|-------------|------------------|-------------|--------------|---|--------------|--------------------------|
| TET | 2200 | - | 12 | - | 086 | x | A | Option Code |
| Product Family | Power Level | Dash | V1 Output | Dash | Width | Airflow | Input | |
| TET Front-End | 2200 W | | 12 V | | 86.3 mm | N: Normal ¹⁾ R: Reverse ²⁾ | A: AC | Blank: Standard model |

¹⁾ Rear to front ²⁾ Front to rear

2. OVERVIEW

The TET2200-12-086 Series is a fully DSP controlled, highly efficient front-end power supply. It incorporates resonant-soft-switching technology and interleaved power trains to reduce component stresses, providing increased system reliability and very high efficiency. With a wide input operating voltage range and minimal linear derating of output power with respect to ambient temperature, the TET2200-12-86NA maximizes power availability in demanding server, switch, and router applications. The power supply is fan cooled and ideally suited for server integration with a matching airflow path.

The PFC stage is digitally controlled using a state-of-the-art digital signal processing algorithm to guarantee best efficiency and unity power factor over a wide operating range.

The DC-DC stage uses soft switching resonant techniques in conjunction with synchronous rectification. An active OR-ing device on the output ensures no reverse load current and renders the supply ideally suited for operation in redundant power systems. The always-on +12V standby output provides power to external power distribution and management controllers. Its protection with an active OR-ing device provides for maximum reliability.

Status information is provided with front-panel LED. In addition, the power supply can be monitored and controlled (i.e. fan speed setpoint) via I2C communication interface with Power Management Bus protocol. It allows full monitoring of the supply, including input and output voltage, current, power, and inside temperatures. The same I2C bus supports the bootloader to allow field update of the firmware in the DSP controllers.

Cooling is managed by a fan, controlled by the DSP controller. The fan speed is adjusted automatically depending on the actual power demand and supply temperature and can be overridden through the I2C buses.

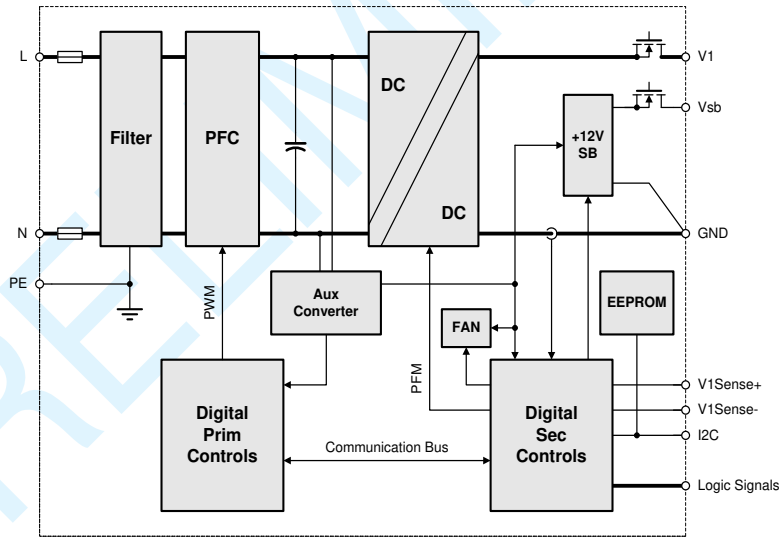


Figure 1. TET2200-12-086 Series Block Diagram

3. ABSOLUTE MAXIMUM RATINGS

Stresses in excess of the absolute maximum ratings may cause performance degradation, adversely affect long-term reliability and cause permanent damage to the supply.

| PARAMETER | CONDITIONS / DESCRIPTION | | MIN | MAX | UNITS |
|---------------------------|--------------------------|------------|-----|-----|-------|
| <i>V_{i maxc}</i> | Maximum Input | Continuous | | 264 | VAC |



Asia-Pacific Europe, Middle East North America
 +86 755 298 85888 +353 61 225 977 +1 408 785 5200

4. INPUT

General Condition: $T_A = 0 \dots +55 \text{ }^\circ\text{C}$, unless otherwise noted.

| PARAMETER | DESCRIPTION / CONDITION | MIN | NOM | MAX | UNIT | |
|-------------------------|--------------------------------------|--|-------|------|------------------|----|
| $V_{i \text{ nom}}$ | AC Nominal Input Voltage | 100 | 230 | 240 | VAC | |
| V_i | AC Input Voltage Ranges | Normal operating ($V_{i \text{ min}}$ to $V_{i \text{ max}}$) | | 264 | VAC | |
| $V_{i \text{ nom DC}}$ | DC Nominal Input Voltage | Rated HVDC | | 240 | VDC | |
| $V_{i \text{ DC}}$ | DC Input Voltage Ranges | Normal operating ($V_{i \text{ min}}$ to $V_{i \text{ max}}$) | | 300 | VDC | |
| $V_{i \text{ derated}}$ | Derated Input Voltage Range | See section 10.3 | | 180 | VAC | |
| $I_{i \text{ max}}$ | Max Input Current | $V_i > 200 \text{ VAC}, > 100 \text{ VAC}$ | | 15 | A _{rms} | |
| $I_{i \text{ p}}$ | Inrush Current Limitation | $V_{i \text{ min}}$ to $V_{i \text{ max}}, T_{\text{NTC}} = 25^\circ\text{C}$ (See Figure 2) | | 35 | A _p | |
| F_i | Input Frequency | 47 | 50/60 | 63 | Hz | |
| PF | Power Factor | $V_{i \text{ nom}}, 50\text{Hz}, > 0.2 I_{i \text{ nom}}$ | | 0.96 | W/VA | |
| $V_{i \text{ on}}$ | Turn-on Input Voltage ²⁾ | Ramping up | | 90 | VAC | |
| $V_{i \text{ off}}$ | Turn-off Input Voltage ²⁾ | Ramping down | | 85 | VAC | |
| η | Efficiency Without Fan | $V_i = 230 \text{ VAC}, 0.1 \cdot I_{x \text{ nom}}, V_{x \text{ nom}}, T_A = 25^\circ\text{C}$ | | 90 | % | |
| | | $V_i = 230 \text{ VAC}, 0.2 \cdot I_{x \text{ nom}}, V_{x \text{ nom}}, T_A = 25^\circ\text{C}$ | | 94 | | |
| | | $V_i = 230 \text{ VAC}, 0.5 \cdot I_{x \text{ nom}}, V_{x \text{ nom}}, T_A = 25^\circ\text{C}$ | | 96 | | |
| | | $V_i = 230 \text{ VAC}, I_{x \text{ nom}}, V_{x \text{ nom}}, T_A = 25^\circ\text{C}$ | | 91 | | |
| T_{hold} | Hold-up Time | After last AC 45C degree (Worst case), $V_i > 11.7\text{V}, V_{\text{SB}}$ within regulation, $V_i = 230 \text{ VAC}, 0.7 P_{x \text{ nom}}$ | | 10 | 11 | ms |

²⁾ The Front-End is provided with a typical hysteresis of 5 V during turn-on and turn-off within the ranges.

4.1 INPUT FUSE

Quick-acting 20 A input fuses (5.4 × 22.5 in mm) in series with the L-line inside the power supply protect against severe defects. The fuses are not accessible from the outside and are therefore not serviceable parts.

4.2 INRUSH CURRENT

The AC-DC power supply exhibits an X-capacitance of only 3.88 μF , resulting in a low and short peak current, when the supply is connected to the mains. The internal bulk capacitor will be charged through a PTC which will limit the inrush current.

NOTE: Do not repeat plug-in / out operations below 5 sec interval time at maximum input, high temperature condition, or else the internal in-rush current limiting device PTC may not sufficiently cool down and excessive inrush current or component failure(s) may result.

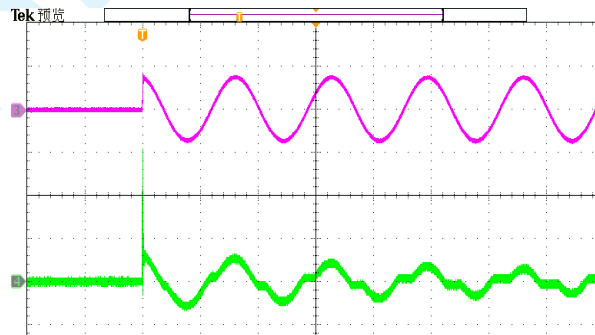


Figure 2. Inrush current, $V_{in} = 264\text{Vac}, 90^\circ$
 CH3: V_{in} (500V/div), CH4: I_{in} (10A/div)

4.3 INPUT UNDER-VOLTAGE

If the RMS value of input voltage (either AC or DC) stays below the input undervoltage lockout threshold V_{on} , the supply will be inhibited. Once the input voltage returns within the normal operating range, the supply will return to normal operation again.

4.4 POWER FACTOR CORRECTION

Power factor correction (PFC) (see *Figure 3*) is achieved by controlling the input current waveform synchronously with the input voltage. A fully digital controller is implemented giving outstanding PFC results over a wide input voltage and load ranges. The input current will follow the shape of the input voltage. If for instance the input voltage has a trapezoidal waveform, then the current will also show a trapezoidal waveform. At DC input voltage the PFC is still in operation, but the input current will be DC in this case.

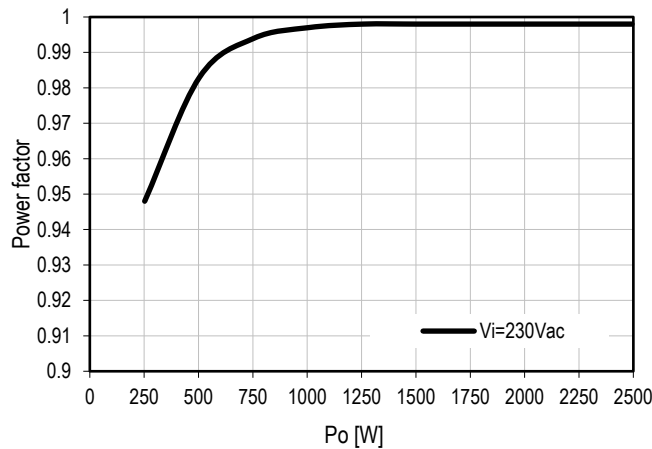


Figure 3. Power Factor vs. Load

4.5 EFFICIENCY

The high efficiency (see *Figure 4*) is achieved by using state-of-the-art GaN power devices in conjunction with soft-transition topologies minimizing switching losses and a full digital control scheme. Synchronous rectifiers on the output reduce the losses in the high current output path. The rpm of the fan is digitally controlled to keep all components at an optimal operating temperature regardless of the ambient temperature and load conditions.

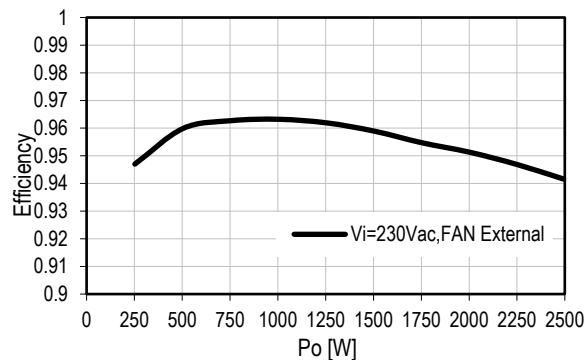


Figure 4. Efficiency vs. Load

5. OUTPUT

General Condition: $T_a = 0 \dots +55^\circ\text{C}$ unless otherwise specified.

| PARAMETER | DESCRIPTION / CONDITION | MIN | NOM | MAX | UNIT |
|--|------------------------------|--|------|--------|-----------------------|
| Main Output V_1 | | | | | |
| $V_{1\text{ nom}}$ | Nominal Output Voltage | | 12.2 | | VDC |
| $V_{1\text{ set}}$ | Output Setpoint Accuracy | $0.5 \cdot I_{1\text{ nom}}$, $T_{\text{amb}} = 25^\circ\text{C}$ | | +0.5 | % $V_{1\text{ nom}}$ |
| $dV_{1\text{ tot}}$ | Total Regulation | $V_{1\text{ min}}$ to $V_{1\text{ max}}$, 0 to 100% $I_{1\text{ nom}}$, $T_{a\text{ min}}$ to $T_{a\text{ max}}$ | | +2 | % $V_{1\text{ nom}}$ |
| $P_{1\text{ nomll}}$ | Nominal Output Power | $V_1 = 12.2\text{ VDC}$, $V_{\text{in}} < 180\text{ VAC}$ | 1200 | | W |
| $I_{1\text{ nomll}}$ | Nominal Output Current | $V_1 = 12.2\text{ VDC}$, $V_{\text{in}} < 180\text{ VAC}$ | 100 | | A |
| $I_{1\text{ ol1}}$ | Over load 1 | $V_1 = 12.2\text{ VDC}$, $V_{\text{in}} < 180\text{ VAC}$ $T_{a\text{ min}}$ to $T_{a\text{ max}}$, Latching ¹ after maximum duration 20s | 120 | | A |
| $I_{1\text{ ol2}}$ | Over load 2 | $V_1 = 12.2\text{ VDC}$, $V_{\text{in}} < 180\text{ VAC}$ $T_{a\text{ min}}$ to $T_{a\text{ max}}$, Latching ¹ after maximum duration 20ms | 140 | | A |
| $P_{1\text{ nom}}$ | Nominal Output Power | $V_1 = 12.2\text{ VDC}$, $V_{\text{in}} > 180\text{ VAC}$ | 2200 | | W |
| $I_{1\text{ nom}}$ | Nominal Output Current | $V_1 = 12.2\text{ VDC}$, $V_{\text{in}} > 180\text{ VAC}$ | 183 | | A |
| $I_{1\text{ hl ol1}}$ | Over load 1 | $V_1 = 12.2\text{ VDC}$, $V_{\text{in}} > 180\text{ VAC}$ $T_{a\text{ min}}$ to $T_{a\text{ max}}$, Latching ¹ after maximum duration 20s | 219 | | A |
| $I_{1\text{ hl ol2}}$ | Over load 2 | $V_1 = 12.2\text{ VDC}$, $V_{\text{in}} > 180\text{ VAC}$ $T_{a\text{ min}}$ to $T_{a\text{ max}}$, Latching ¹ after max. duration 20 ms | 256 | | A |
| $I_{1\text{ ol}}$ | Short Time Over Load Current | $V_1 = 12.2\text{VDC}$, $T_{a\text{ min}}$ to $T_{a\text{ max}}$, immediate shutdown | 310 | | A |
| $V_{1\text{ pp}}$ | Output Ripple Voltage | $V_{1\text{ nom}}$, $I_{1\text{ nom}}$, 20MHz BW (See Section 5.1) (see Figure 11, 12) | 90 | 120 | mVpp |
| $dV_{1\text{ Load}}$ | Load Regulation | $V_1 = V_{1\text{ nom}}$, 0 - 100 % $I_{1\text{ nom}}$ | 140 | | mV |
| $dV_{1\text{ Line}}$ | Line Regulation | $V_1 = V_{1\text{ min}} \dots V_{1\text{ max}}$ | 0 | | mV |
| dI_{share} | Current Sharing | $(I_x - I_y) / I_{\text{tot}}$, $I > 25\%$ $I_{1\text{ nom}}$ | -5 | +5 | % |
| dV_{dyn} | Dynamic Load Regulation | $\Delta I = 50\%$ $I_{1\text{ nom}}$, $I = 5 \dots 100\%$ $I_{1\text{ nom}}$, $dI/dt = 1\text{A}/\mu\text{s}$, recovery within 1% of $V_{1\text{ nom}}$ (see Figure 13, 14, 15, 16) | -0.6 | 0.6 | V |
| T_{rec} | Recovery Time | | 0.5 | 1 | ms |
| $t_{\text{AC } V_1}$ | Start-up Time from AC | $V_1 = 10.8\text{ VDC}$ (see Figure 5) | | 2 | sec |
| $t_{V_1\text{ rise}}$ | Rise Time | $V_1 = 10 \dots 90\%$ $V_{1\text{ nom}}$ (see Figure 8) | | 20 | ms |
| C_{Load} | Capacitive Loading | $T_a = 25^\circ\text{C}$ | | 50,000 | μF |
| Standby Output V_{SB} | | | | | |
| $V_{\text{SB nom}}$ | Nominal Output Voltage | | 12.0 | | VDC |
| $V_{\text{SB set}}$ | Output Setpoint Accuracy | $0.5 \cdot I_{\text{SB nom}}$, $T_{\text{amb}} = 25^\circ\text{C}$ | | +1 | % $V_{\text{SB nom}}$ |
| $dV_{\text{SB tot}}$ | Total Regulation | $V_{1\text{ min}}$ to $V_{1\text{ max}}$, 0 to 100% $I_{\text{SB nom}}$, $T_{a\text{ min}}$ to $T_{a\text{ max}}$ | | +3 | % $V_{\text{SB nom}}$ |
| $P_{\text{SB nom}}$ | Nominal Output Power | $V_{\text{SB}} = 12.0\text{ VDC}$ | 42 | | W |
| $I_{\text{SB nom}}$ | Nominal Output Current | $V_{\text{SB}} = 12.0\text{ VDC}$ | 3.5 | | A |
| $I_{\text{SB ol1}}$ | Over load 1 | Hiccup for both output after 20s | 4 | 4.5 | A |
| $I_{\text{SB ol2}}$ | Over load 2 | Hiccup for 12VSB after 15ms | 4.5 | | A |
| $V_{\text{SB pp}}$ | Output Ripple Voltage | $V_{\text{SB nom}}$, $I_{\text{SB nom}}$, 20 MHz BW (See Section 5.1) (see Figure 9, 10) | 60 | 120 | mVpp |
| dV_{SB} | Droop | 0 - 100 % $I_{\text{SB nom}}$ | 180 | | mV |
| $dV_{\text{SB dyn}}$ | Dynamic Load Regulation | $\Delta I_{\text{SB}} = 50\%$ $I_{\text{SB nom}}$, $I_{\text{SB}} = 5 \dots 100\%$ $I_{\text{SB nom}}$, $dI/dt = 1\text{A}/\mu\text{s}$, recovery within 1% of $V_{1\text{ nom}}$ | -0.6 | 0.6 | V |
| T_{rec} | Recovery Time | | | 0.5 | ms |
| $t_{\text{AC } V_{\text{SB}}}$ | Start-up Time from AC | $V_{\text{SB}} = 90\%$ $V_{\text{SB nom}}$ (see Figure 5) | | 2 | sec |
| $t_{V_{\text{SB}}\text{ rise}}$ | Rise Time | $V_{\text{SB}} = 10 \dots 90\%$ $V_{\text{SB nom}}$ (see Figure 7) | | 20 | ms |
| C_{Load} | Capacitive Loading | $T_{\text{amb}} = 25^\circ\text{C}$ | | 3,100 | μF |

¹ Latch-off requires elimination of fault condition and then recycling either the AC input or PS_ON recycle to resume operation

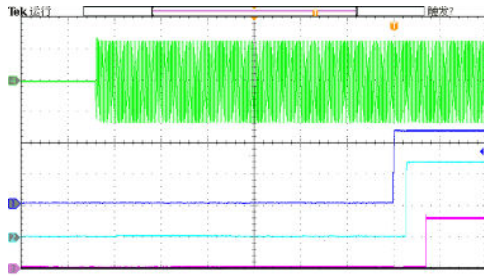


Figure 5. Turn-On AC Line 230VAC, full load (400ms/div)

CH1: V_{SB} (5V/div) CH2: V_1 (5V/div)
CH3: PWOK (2V/div) CH4: V_{in} (250V/div)

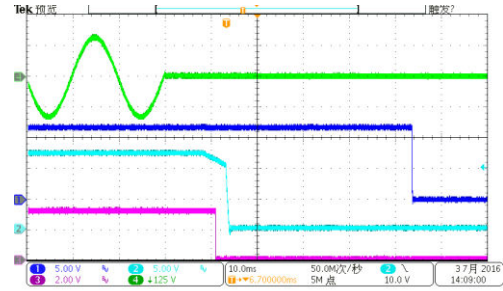


Figure 6. Turn-Off AC Line 230VAC, full load (10ms/div)

CH1: V_{SB} (5V/div) CH2: V_1 (5V/div)
CH3: PWOK (2V/div) CH4: V_{in} (250V/div)

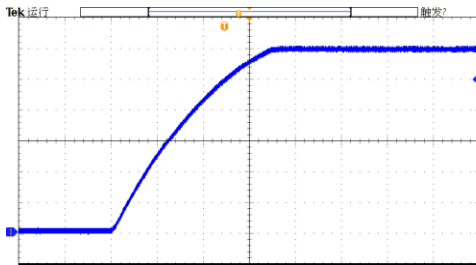


Figure 7. Turn-On AC Line 230VAC, full load (4ms/div)

CH1: V_{SB} (2V/div)

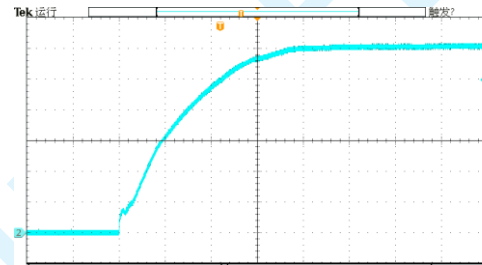


Figure 8. Turn-On AC Line 230VAC, full load (2ms/div)

CH2: V_1 (2V/div)

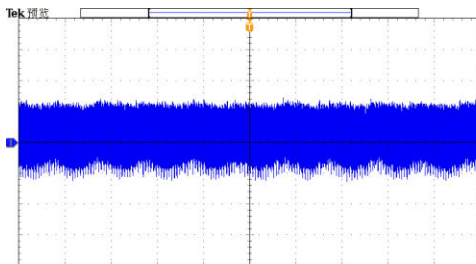


Figure 9. V_{SB} Ripple 230VAC, full load (10ms/div)

CH1: V_{SB} (20mV/div)

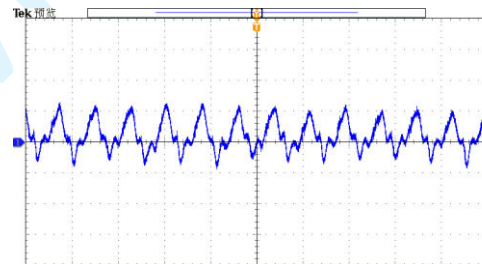


Figure 10. V_{SB} Ripple 230VAC, full load (10us/div)

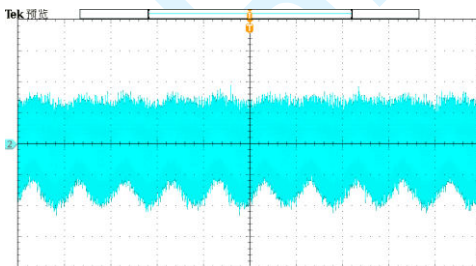


Figure 11. V_1 Ripple 230VAC, full load (10ms/div)

CH2: V_1 (20mV/div)

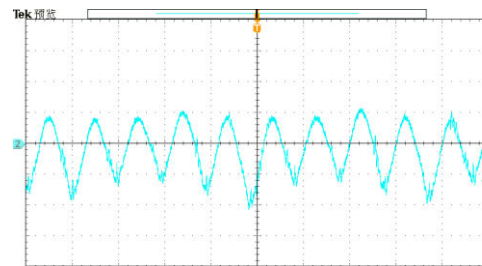


Figure 12. V_1 Ripple 230VAC, full load (2us/div)

CH2: V_1 (20mV/div)

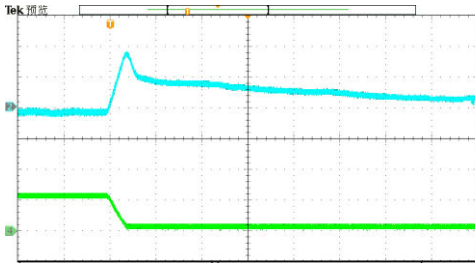


Figure 13. Load Transient V1, 111.65 to 10.15 A, 1A/uS (200 μs/div)
CH2: V₁ (200mV/div) CH4: I₁ (100A/div)

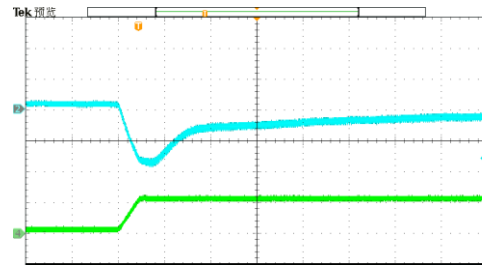


Figure 14. Load Transient V1, 10.15 to 111.65 A, 1A/uS (200 μs/div)
CH2: V₁ (200mV/div) CH4: I₁ (100A/div)

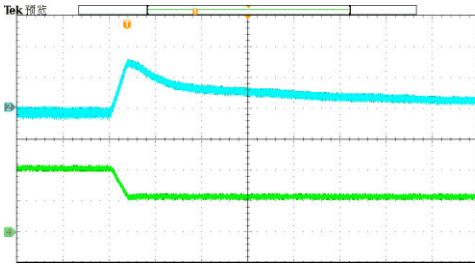


Figure 15. Load Transient V1, 203 to 101.5 A, 1A/uS (200 μs/div)
CH2: V₁ (200mV/div) CH4: I₁ (100A/div)

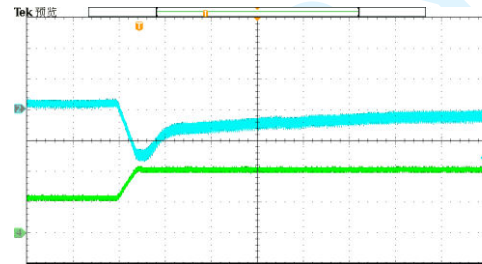


Figure 16. Load Transient V1, 101.5 to 203 A, 1A/uS (200 μs/div)
CH2: V₁ (200mV/div) CH4: I₁ (100A/div)

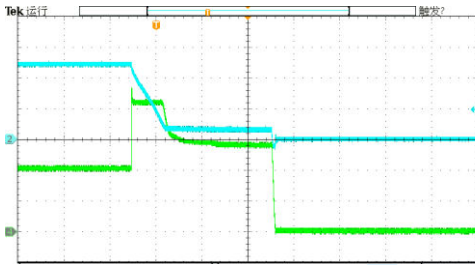


Figure 17. Short circuit on V1 (4ms/Div), Short with 400A
CH2: V₁ (5V/div) CH4: I₁ (100A/div)

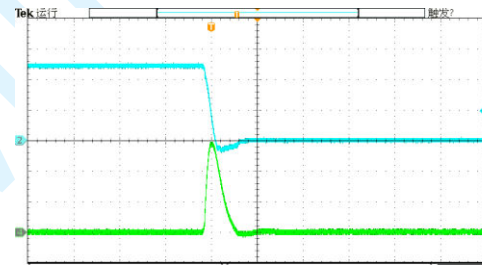


Figure 18. Short circuit on V1 (0.4ms/Div), Short without control
CH2: V₁ (5V/div) CH4: I₁ (500A/div)

5.1 OUTPUT VOLTAGE RIPPLE

Ripple and noise shall be measured using the following methods:

- Outputs bypassed at the point of measurement with a parallel combination of 10μF tantalum capacitor in parallel with 0.1μF ceramic capacitors, referring the setup in Figure 19.
- The ripple voltage is measured with 20 MHz BWL.

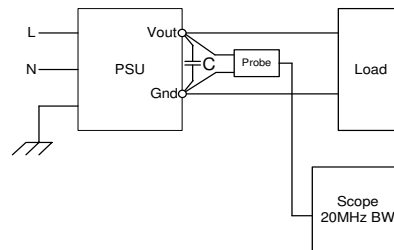


Figure 19. Output Ripple Test Setup

5.2 SHORT TIME OVERLOAD

The main output has the capability to allow load current up to 40% above the nominal output current rating for a maximum duration of 20ms. This allows the system to consume extended power for short time dynamic processes.

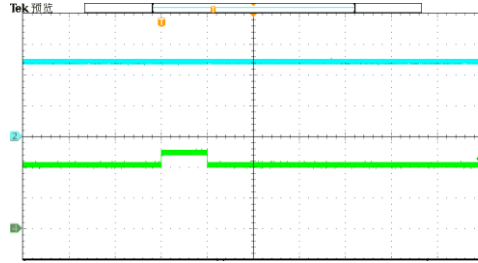


Figure 20. Short circuit on V1 (20ms/Div)
CH2: V_i (5V/div) CH4: I_{in} (100A/div)

5.3 OUTPUT GROUND / CHASSIS CONNECTION

The output return path serves as power and signal ground. All output voltages and signals are referenced to these pins. To prevent a shift in signal and voltage levels due to ground wiring voltage drop a low impedance ground plane should be used as shown in Figure 21. Alternatively, separated ground signals can be used as shown in Figure 22. In this case the two ground planes should be connected at the power supplies ground pins.

NOTE: Within the power supply the output GND pins are connected to the Chassis, which in turn is connected to the Protective Earth terminal on the AC inlet. Therefore, it is not possible to set the potential of the output return (GND) to any other than Protective Earth potential.

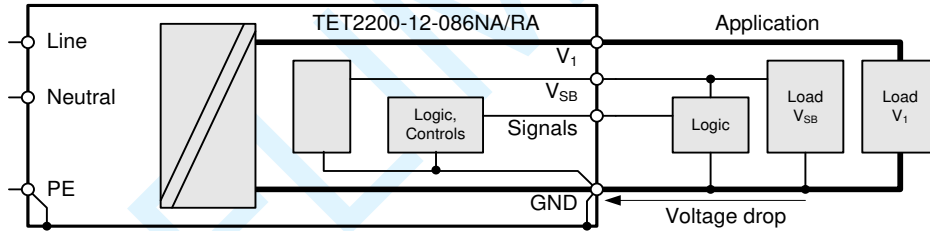


Figure 21. Common Low Impedance Ground Plane

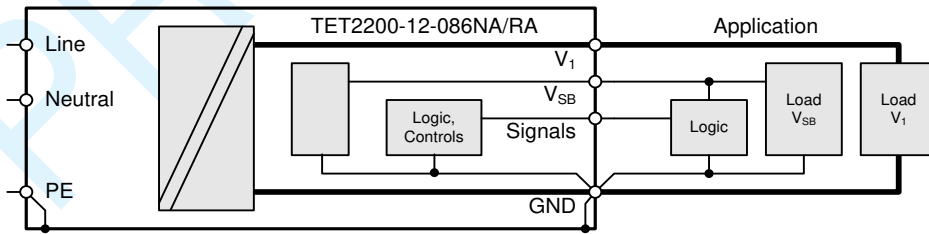


Figure 22. Separated Power and Signal Ground

6. PROTECTION SPECIFICATIONS

| PARAMETER | DESCRIPTION / CONDITION | MIN | NOM | MAX | UNIT | |
|--------------------------------|--|---|------------|-------------------|------------|---|
| F | Input Fuse (Line) | Not user accessible, quick-acting (F) | | 20 | A_{rms} | |
| $V_{1\text{ OV}}$ | OV Threshold V_1 | 13.3 | 13.9 | 14.5 | VDC | |
| $t_{\text{OV } V_1}$ | OV Latch Off Time V_1 | | | 1 | ms | |
| $V_{\text{SB OV}}$ | OV Threshold V_{SB} | 13.3 | 13.9 | 14.5 | VDC | |
| $t_{\text{OV } V_{\text{SB}}}$ | OV Latch Off Time V_{SB} | | | 1 | ms | |
| $I_{1\text{ lim}}$ | Current Limitation I_1 | $I_1 < 180\text{ VAC}$ $I_1 > 180\text{ VAC}$ | 105 194 | 107 196 | 109 198 | A |
| $t_{1\text{ lim}}$ | Current Limit Blanking Time | Time to latch off when in over current | | 20 | ms | |
| $I_{1\text{ ol lim}}$ | Current Limit During Short Time Overload I_1 | Maximum duration 20 ms | | 256 | A | |
| $I_{1\text{ SC}}$ | Max Short Circuit Current I_1 | $V_1 < 3\text{ V}$ | | 300 ³⁾ | A | |
| $t_{1\text{ SC off}}$ | Short Circuit Latch Off Time | Time to latch off when in short circuit (Short circuit current < 400 A) See Figure 17 (Short circuit current > 400 A) See Figure 18 | | 10 0.2 | ms | |
| $I_{\text{SB lim}}$ | Current Limitation V_{SB} | | 4.1 | | A | |
| $t_{\text{SB lim}}$ | Current Limit Blanking Time | Time to hit hiccup when in over current | | 1 | ms | |

³⁾ Limit set doesn't include effects of main output capacitive discharge.

6.1 OVERVOLTAGE PROTECTION

The TET2200-12-086 Series front-end provides a fixed threshold overvoltage (OV) protection implemented with a HW comparator for both the main and the standby output. Once an OV condition has been triggered on the main output, the supply will shut down and latch the fault condition. The latch can be unlocked by disconnecting the supply from the AC mains or by toggling the PSON_L input. The standby output will continuously try to restart with a 1 s interval after OV condition has occurred.

6.2 UNDERVOLTAGE DETECTION

Both main and standby outputs are monitored. PWOK pin signal if the output voltage exceeds $\pm 5\%$ of its nominal voltage. The main output will latch off if the main output voltage when V_1 falls below 11.2V (typically in an overload condition), the latch can be unlocked by disconnecting the supply from the AC mains or by toggling the PSON_L input. If the standby output leaves its regulation bandwidth for more than 10ms then the main output is disabled to protect the system, and the standby output will continuously try to restart with a 1s interval after UV condition has occurred.

| PARAMETER | DESCRIPTION / CONDITION | MIN | NOM | MAX | UNIT | |
|---------------------|-------------------------|---|-----|------|------|---|
| $V_{1\text{ mon}}$ | Input RMS Voltage | $V_{1\text{ min}} \leq V_1 \leq V_{1\text{ max}}$ | | -2.5 | +2.5 | % |
| $I_{1\text{ mon}}$ | Input RMS Current | $I_1 > 6\text{ A}_{rms}$ $I_1 \leq 6\text{ A}_{rms}$ | | -5 | +5 | % |
| $P_{1\text{ mon}}$ | True Input Power | $P_1 > 700\text{ W}$ $P_1 \leq 700\text{ W}$ | | -5 | +5 | % |
| $V_{1\text{ mon}}$ | V_1 Voltage | | | -2 | +2 | % |
| $I_{1\text{ mon}}$ | V_1 Current | $I_1 > 30\text{ A}$ $I_1 \leq 30\text{ A}$ | | -2 | +2 | % |
| $P_{1\text{ mon}}$ | Total Output Power | $P_o > 200\text{ W}$ $P_o \leq 200\text{ W}$ | | -5 | +5 | % |
| $V_{\text{SB mon}}$ | Standby Voltage | | | -2 | +2 | % |
| $I_{\text{SB mon}}$ | Standby Current | $I_{\text{SB}} \leq I_{\text{SB nom}}$ | | -0.2 | +0.2 | A |

Table 1. Monitoring accuracy

7. SIGNALING AND CONTROL

8.1 ELECTRICAL CHARACTERISTICS (INPUT SIGNALS)

All Input signals versus signal ground SGND pin of output connector in PSU

| PARAMETER | DESCRIPTION | MIN | NOM | MAX | UNIT |
|-------------------------------|--|---------------------|-----|------|------------|
| PSKILL / PSON_L inputs | | | | | |
| V_L | Input low level voltage | -0.2 | | 0.5 | V |
| V_H | Input high level voltage | 2.0 | | 5.25 | V |
| $I_{L, H}$ | Maximum input sink or source current | VI = -0.2V to +3.5V | | 4 | mA |
| $R_{puPSKILL}$ | Internal pull up resistor to internal 3.3V on PSKILL | | 10 | | k Ω |
| R_{puPSON_L} | Internal pull up resistor to internal 3.3V on PSON_L | | 10 | | k Ω |

Table 2. Input signals

8.1.1 PSKILL INPUT

The PSKILL input is an active-high and normally a trailing pin in the connector and is used to disconnect the main output as soon as the power supply is being plugged out. This pin should be connected to SGND on the system. The standby output will remain on regardless of the PSKILL input state.

8.1.2 PSON_L INPUT

The PSON_L is an internally pulled-up (3.3V) input signal via 10kohm resistor to enable / disable the main output V1 of the front-end. This active-low pin is also used to clear any latched fault condition. Figure 26 shows PSON_L circuit used in PSU and proposed connections.

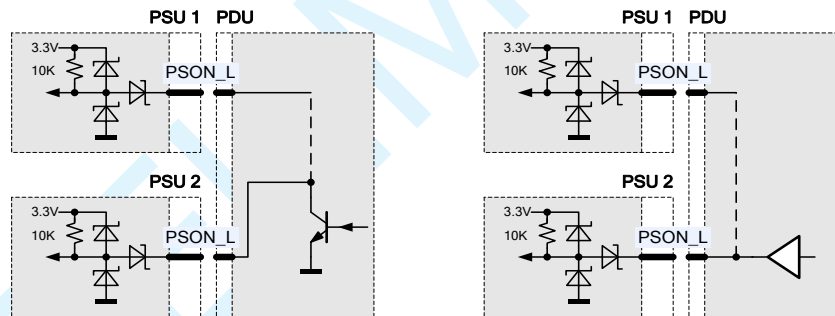


Figure 26. PSON_L Connection

8.1.3 SENSE INPUTS

The main output has sense lines implemented to compensate for voltage drop on load wires in both positive and negative path. The maximum allowed voltage drop is 200 mV on the positive rail and 50 mV on the GND rail.

With open sense inputs the main output voltage will rise by 250 mV. Therefore, if not used, these inputs should be connected to the power output and GND at the power supply connector. The sense inputs are protected against short circuit. In this case the power supply will shut down.

8.2 ELECTRICAL CHARACTERISTICS (OUTPUT SIGNALS)

All Output signals versus signal ground SGND in PSU.

| PARAMETER | DESCRIPTION | MIN | NOM | MAX | UNIT |
|---------------------------|---|--|-----------|----------|------------|
| PWOK output | | | | | |
| V_{OL} | Output low level voltage | V1 or VSB out of regulation $I_{sink}=400\mu A$ | 0 | 0.4 | V |
| V_{OH} | Output high level voltage | V1 and VSB in regulation $I_{source}=200\mu A$ | 2.4 | 3.46 | V |
| I_{OL} | Maximum Sink Current | PWOK = low | | 400 | μA |
| I_{OH} | Maximum Source Current | PWOK = high | | 2 | mA |
| R_{puPWOK} | Recommended external pull up resistor on PWOK at $V_{puPWOK} = 3.3 V$ $V_{puPWOK} = 5 V$ | | 6.8 10 | 10 15 | k Ω |
| ACOK output | | | | | |
| V_{OL} | Output low level voltage | $I_{sink} < 4mA$ | 0 | 0.4 | V |
| V_{OH} | Output high level voltage | | 2.4 | 3.46 | V |
| R_{puACOK} | An internal pull up resistor on ACOK at $V_{puACOK} = 3.3 V$ | | 1 | | k Ω |
| <i>Low level output</i> | Input voltage is not within range for PSU to operate | | 0 | 0.4 | V |
| <i>High level output</i> | Input voltage is within range for PSU to operate | | 2.4 | 3.46 | V |
| SMB_ALERT_L output | | | | | |
| V_{OL} | Output low level voltage | $I_{sink} < 4 mA$ | 0 | 0.4 | V |
| V_{OH} | Output open collector | | 2.4 | 3.46 | V |
| $R_{puSMB_ALERT_L}$ | An internal pull up resistor on SMB_ALERT_L at $V_{puSMB_ALERT_L} = 3.3V$ | | 10 | | k Ω |
| <i>Low level output</i> | PSU in warning or failure condition | | | | |
| <i>High level output</i> | PSU is ok | | | | |
| PRESENT_L output | | | | | |
| V_{OL} | Output low level voltage | $I_{sink} < 4 mA$ | 0 | 0.4 | V |
| V_{OH} | N.A | This pin is shorted to SGND via 100ohm resistor in PSU | | | V |
| $R_{puPRESENT_L}$ | Recommended external pull up resistor on PRESENT_L at $V_{puPRESENT_L} = 3.3V$ | | 10 | | k Ω |
| <i>Low level output</i> | PSU is present | | | | |
| <i>High level output</i> | PSU is not present | | | | |

Table 3. Output signals

8.2.1 PWOK

PWOK is a power OK signal and will be pulled HIGH by the power supply to indicate that all the outputs are within the regulation limits of the power supply. When any output voltage falls below regulation limits or when AC power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, PWOK will be de-asserted to a LOW state.

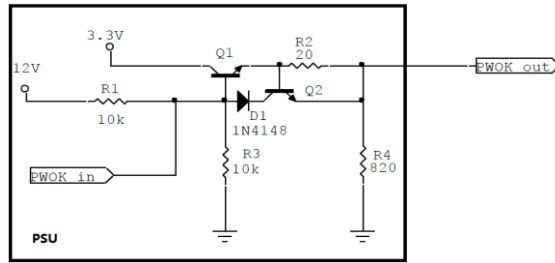


Figure 27. PWOK circuit in PSU

8.2.2 ACOK

The ACOK is an internal pull-up to 3.3V via 1kohm resistor indicating whether the input is within the range the power supply can use and turn on. A 15V zener diode is added on this signal pin versus signal ground SGND to protect internal circuits from negative and high positive voltage. The ACOK signal is active-high.

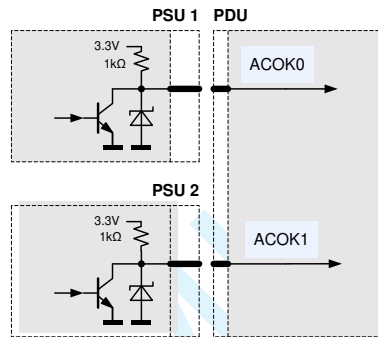


Figure 28. ACOK Connection

8.2.3 SMB_ALERT_L

The SMB_ALERT_L is an internal pull-up to 3.3V via 10kohm resistor indicating the power supply is experiencing a problem that the system agent should investigate. This is a logical OR of the Shutdown and Warning events. It is asserted (pulled Low) at Shutdown or Warning events such as reaching temperature warning/shutdown threshold of critical component, general failure, over-current, over-voltage, under-voltage or low-speed of failed fan. This signal may also indicate the power supply is operating in an environment exceeding the specified limits. This signal is to be asserted in parallel with LED turning solid Amber.

The power supply shall assert the over temperature SMB_ALERT_L signal when a hot spot or inlet temperature sensor crosses a warning threshold. The inlet temperature warning threshold must be set at 57.5°C(NA) and 62°C(RA), preventing exhaust air and cord temperatures exceeding safety ratings. The warning gets deserted once inlet air temperature returns into specified operating temperature range. Fan speed control algorithm shall ramp up the fan speed to the maximum prior to the SMB_ALERT_L insertion. A 15V zener diode is added on this signal pin versus signal ground SGND to protect internal circuits from negative and high positive voltage.

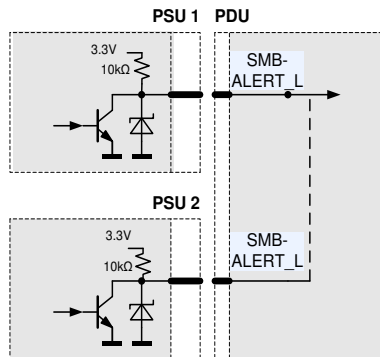


Figure 29. SMB_ALERT_L Connection

8.2.4 PRESENT_L OUTPUT

The PRESENT_L pin is wired to internal SGND within the power supply. This pin does indicate that there is a power supply present in this system slot. An external pull-up resistor has to be added within the application. Current into PRESENT_L should not exceed 4 mA to guarantee a low level voltage if power supply is seated.

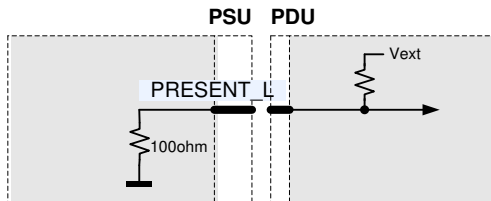


Figure 30. PRESENT_L Signal Pin

8.3 ELECTRICAL CHARACTERISTICS (BIDIRECTIONAL SIGNALS)

8.3.1 CURRENT SHARE

All Output signals versus signal ground SGND in PSU

The TET front-ends have an active current share scheme implemented for V1. All the ISHARE current share pins need to be interconnected in order to activate the sharing function. If a supply has an internal fault or is not turned on, it will disconnect its ISHARE pin from the share bus. This will prevent dragging the output down (or up) in such cases.

The current share function uses an analog bus to transmit and receive current share information. The controller implements a Master/Slave current share function. The power supply providing the largest current among the group is automatically the Master. The other supplies will operate as Slaves and increase their output current to a value close to the Master by slightly increasing their output voltage. The voltage increase is limited to +250 mV. The output will share within 5% at full load.

ISHARE pins must be interconnected without any additional components. This in-/output has a 15 V zener diode as a protection device and is disconnected from internal circuits when the power supply is switched off.

The 12VSB output is not required to actively share current between power supplies (passive sharing).

| No of paralleled PSUs | Maximum available power on main 12V without redundancy | Maximum available power on main 12V with n+1 redundancy | Maximum available power standby output |
|-----------------------|--|---|--|
| 1 | 2200 W | - | 42 W |
| 2 | 4290 W | 2200 W | 42 W |
| 3 | 6435 W | 4290 W | 42 W |
| 4 | 8580 W | 6435 W | 42 W |
| 5 | 10725 W | 8580 W | 42 W |
| 6 | 12870 W | 10725 W | 42 W |

Table 4. Power Available When PSU in Redundant Operation

8.4 FRONT LEDS

The front-end has 1 front LED showing the status of the supply. LED is bi-colored: green and yellow, and indicates DC power presence or fault situations. For the position of the LED see Table lists the different LED status.

| OPERATING CONDITION | LED State |
|--|--------------------|
| Output ON and OK | Solid GREEN |
| No AC power to all power supplies | OFF |
| AC cord unplugged, or AC power lost; with a second power supply in parallel still with AC input power. | OFF |
| AC present / Only 12 VSB on (Standby mode) | 0.5 Hz Blink GREEN |
| Sleep PS in Smart redundant state/off line mode | 2 Hz Blink GREEN |
| Power supply critical event causing a shutdown; eg. OCP, OVP, OTP, Fan Fail | Solid AMBER |
| Power supply in FW upload mode | 2 Hz Blink GREEN |

Table 5. LED Status

8.5 SIGNAL TIMING

| OPERATING CONDITION | | MIN | MAX | UNIT |
|----------------------|---|-----|------|------|
| $t_{AC VSB}$ | AC Line to 90% V_{SB} | | 2 | sec |
| $t_{AC V1}$ | AC Line to 90% V_1 | | 2 | sec |
| $t_{ACOK on1}$ | ACOK signal on delay (start-up) | | 1700 | ms |
| $t_{ACOK on2}$ | ACOK signal on delay (dips) | 0 | 100 | ms |
| $t_{V1 holdup}$ | Effective V_1 holdup time $P_o < 0.7 P_{x nom}$ | 10 | 300 | ms |
| | Effective V_1 holdup time $P_o > 0.7 P_{x nom}$ | 8 | 300 | ms |
| $t_{VSB holdup}$ | Effective V_{SB} holdup time | 40 | 300 | ms |
| $t_{ACOK V1}$ | ACOK to V_1 holdup $P_o < 0.7 P_{x nom}$ | 7 | | ms |
| | ACOK to V_1 holdup $P_o > 0.7 P_{x nom}$ | 5 | | ms |
| $t_{ACOK VSB}$ | ACOK to V_{SB} holdup | 25 | | ms |
| $t_{V1 off}$ | Minimum V_1 off time | 500 | | ms |
| $t_{VSB off}$ | Minimum V_{SB} off time | 500 | | ms |
| $t_{V1 dropout}$ | Minimum V_1 dropout time | 10 | | ms |
| $t_{VSB dropout}$ | Minimum V_{SB} dropout time | 40 | | ms |
| $t_{V1 rise}$ | V_1 rise time | | 20 | ms |
| $t_{VSB rise}$ | V_{SB} rise time | | 20 | ms |
| $t_{PSON_L V1 on}$ | PSON_L to V_1 Delay (on) | 5 | 350 | ms |
| $t_{PSON_L V1 off}$ | PSON_L to V_1 Delay (off) | 0 | 100 | ms |
| $t_{PWOK del}$ | I_1 to PWOK Delay (on) | 100 | 500 | ms |
| $t_{PWOK warn}$ | PWOK Delay (off) to $V_1 < 11.7 V$ at $P_o < 0.7 P_{x nom}$ | 1 | | ms |
| | PWOK Delay (off) to $V_1 < 11.7 V$ at $P_o > 0.7 P_{x nom}$ | -1 | | ms |

Table 6. Timing

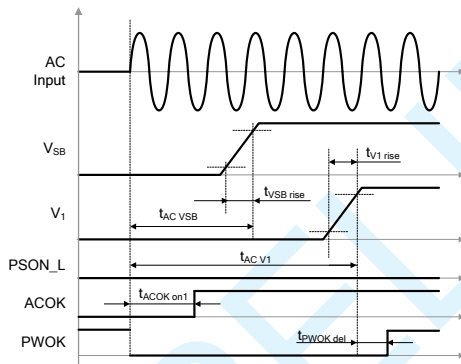


Figure 31. AC Turn-On Timing

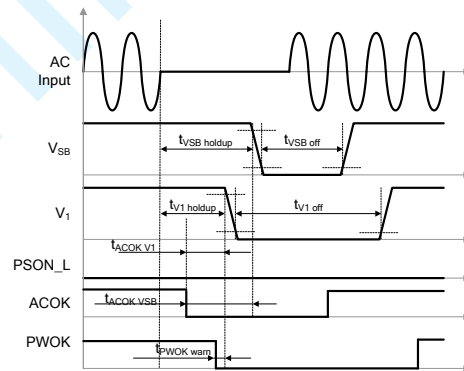


Figure 32. AC Long Dips

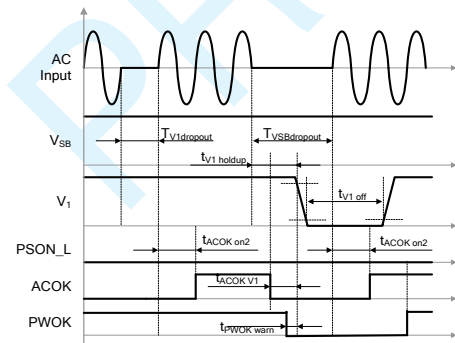


Figure 33. AC Short Dips

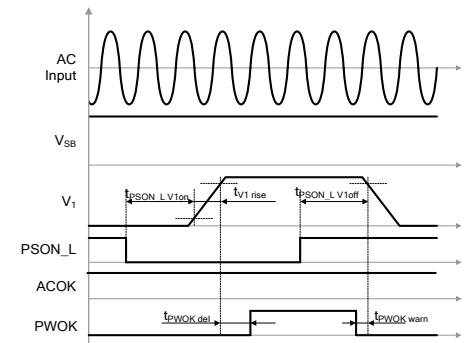


Figure 34. PSON_L Turn-on/off Timing



Asia-Pacific
+86 755 298 85888

Europe, Middle East
+353 61 225 977

North America
+1 408 785 5200

8.6 I2C / POWER MANAGEMENT BUS COMMUNICATION

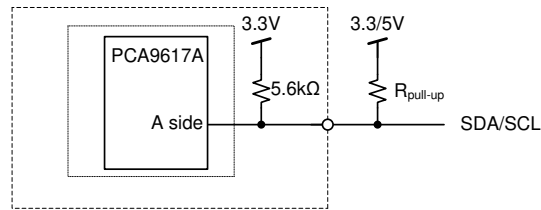


Figure 35. Physical Layer of Communication Interface

The TET front-end is a communication Slave device only; it never initiates messages on the I2C/SMBus by itself. The communication bus voltage and timing is defined in *Table 7* further characterized through:

- The SDA/SCL IOs use 3V3 logic levels
- External pull-up resistors on SDA/SCL required for correct signal edges
- Full SMBus clock speed of 400 kbps
- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognizes any time Start/Stop bus conditions

Communication to the DSP or the EEPROM will be possible as long as the input AC voltage is provided. If no AC is present, communication to the unit is possible if it is connected to a life 12V or 12VSB output (provided e.g. by the redundant unit).

| PARAMETER | DESCRIPTION | CONDITION | MIN | MAX | UNIT |
|------------------|--|---|---------------|---------------------------|---------------|
| SCL / SDA | | | | | |
| V_{iL} | Input low voltage | | -0.5 | 1.0 | V |
| V_{iH} | Input high voltage | | 2.3 | 3.5 | V |
| V_{hys} | Input hysteresis | | 0.15 | | V |
| V_{oL} | Output low voltage | 3 mA sink current | 0 | 0.4 | V |
| t_r | Rise time for SDA and SCL | | $20+0.1C_b^1$ | 300 | ns |
| t_{of} | Output fall time $V_{iHmin} \rightarrow V_{iLmax}$ | $10 \text{ pF} < C_b^1 < 400 \text{ pF}$ | $20+0.1C_b^1$ | 250 | ns |
| I_i | Input current SCL/SDA | $0.1 \text{ VDD} < V_i < 0.9 \text{ VDD}$ | -10 | 10 | μA |
| C_i | Internal Capacitance for each SCL/SDA | | | 0 | pF |
| f_{SCL} | SCL clock frequency | | 0 | 400 | kHz |
| $R_{pull-up}$ | External pull-up resistor | $f_{SCL} \leq 400 \text{ kHz}$ | | $1000 \text{ ns} / C_b^1$ | Ω |
| t_{HDSTA} | Hold time (repeated) START | $f_{SCL} \leq 400 \text{ kHz}$ | 0.6 | | μs |
| t_{LOW} | Low period of the SCL clock | $f_{SCL} \leq 400 \text{ kHz}$ | 1.3 | | μs |
| t_{HIGH} | High period of the SCL clock | $f_{SCL} \leq 400 \text{ kHz}$ | 0.6 | | μs |
| t_{SUSTA} | Setup time for a repeated START | $f_{SCL} \leq 400 \text{ kHz}$ | 0.6 | | μs |
| t_{HDDAT} | Data hold time | $f_{SCL} \leq 400 \text{ kHz}$ | 0 | 0.9 | μs |
| t_{SUDAT} | Data setup time | $f_{SCL} \leq 400 \text{ kHz}$ | 100 | | ns |
| t_{SUSTO} | Setup time for STOP condition | $f_{SCL} \leq 400 \text{ kHz}$ | 0.6 | | μs |
| t_{BUF} | Bus free time between STOP and START | $f_{SCL} \leq 400 \text{ kHz}$ | 1 | | ms |

¹ C_b = Capacitance of bus line in pF, typically in the range of 10...400 pF

Table 7. I2C / SMBus Specification

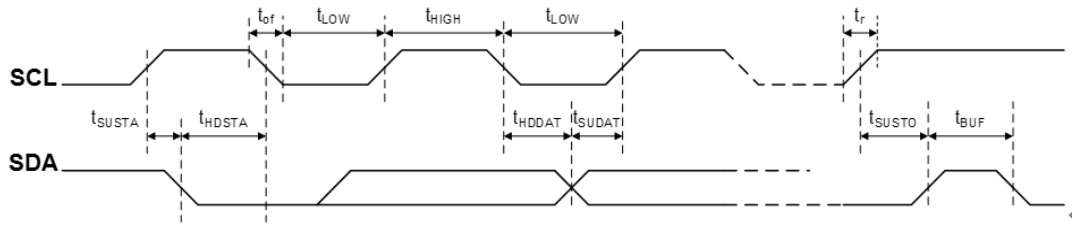


Figure 36. I2C / SMBus Timing

ADDRESS SELECTION

The address for I2C communication can be configured by pulling address input pins A0,A1 and A2 either to GND (Logic Low) or leave them open (Logic High). An internal pull up resistor (10kohm) will cause the A0, A1 and A2 pin to be in High Level if left open. A fixed addressing offset exists between the Controller and the EEPROM.

I2C ADDRESS

| A2 | A1 | A0 | I2C Address | |
|----|----|----|------------------------------|----------------|
| | | | Power Management Bus Address | EEPROM Address |
| 0 | 0 | 0 | 0xB0 | 0xA0 |
| 0 | 0 | 1 | 0xB2 | 0xA2 |

Table 8. Address and Protocol Encoding

8.7 CONTROLLER AND EEPROM ACCESS

The controller and the EEPROM in the power supply share the same I2C bus physical layer (see Figure 37) and can be accessed under different addresses, see Table 8 Address and Protocol Encoding.

The SDA/SCL lines are connected directly to the controller and EEPROM which are supplied by internal 3V3.

The EEPROM provides 256 bytes of user memory. None of the bytes are used for the operation of the power supply.

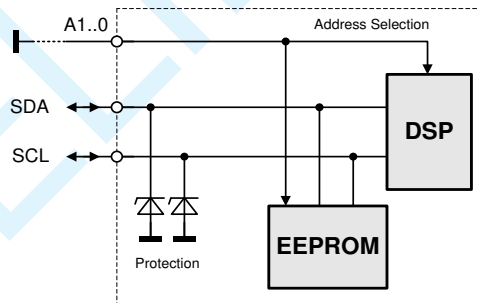


Figure 37. I2C Bus to DSP and EEPROM

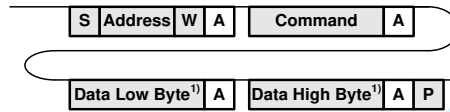
8.9 POWER MANAGEMENT BUS PROTOCOL

The Power Management Bus is an open standard protocol that defines means of communicating with power conversion and other devices. For more information, please see the System Management Interface Forum web site at: www.powerSIG.org. Power Management Bus command codes are not register addresses. They describe a specific command to be executed. TET2200-12-086 Series supply supports the following basic command structures:

- Clock stretching limited to 1 ms
- SCL low time-out of >25 ms with recovery within 10 ms
- Recognized any time Start/Stop bus conditions

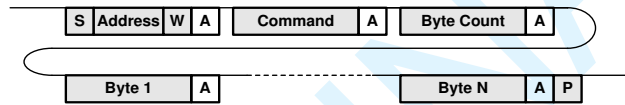
WRITE

The write protocol is the SMBus 1.1 Write Byte/Word protocol. Note that the write protocol may end after the command byte or after the first data byte (Byte command) or then after sending 2 data bytes (Word command).



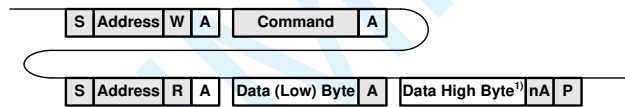
¹) Optional

In addition, Block write commands are supported with a total maximum length of 255 bytes. See TET2200-12-086 Series Programming Manual for further information.



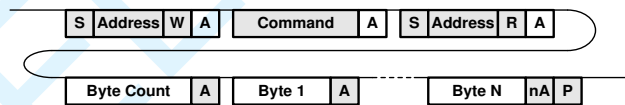
READ

The read protocol is the SMBus 1.1 Read Byte/Word protocol. Note that the read protocol may request a single byte or word.



¹) Optional

In addition, Block read commands are supported with a total maximum length of 255 bytes. See TET2200-12-086 Series Power Management Bus Communication Manual URP.00560 for further information.



8. MECHANICAL SPECIFICATIONS

| PARAMETER | DESCRIPTION / CONDITION | MIN | NOM | MAX | UNIT |
|------------|-------------------------|-----|-------|-----|------|
| Dimensions | Width | | 86.3 | | mm |
| | Height | | 39.3 | | |
| | Depth | | 196.5 | | |
| M | Weight | | 1.2 | | kg |

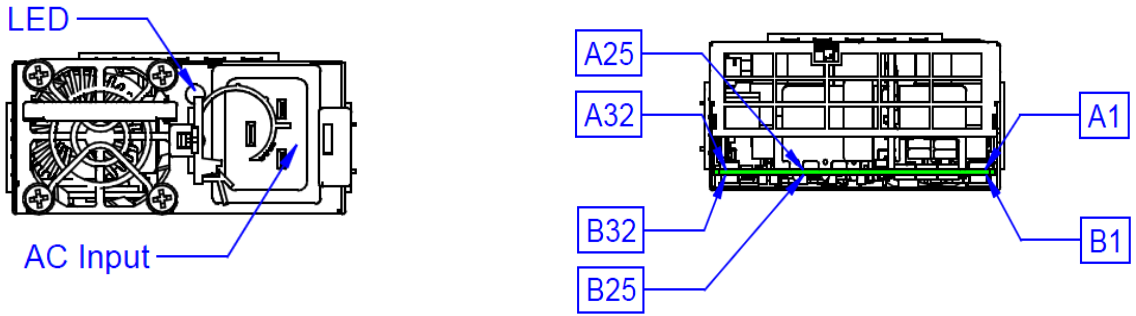


Figure 38. Mechanical Drawing - Front / Rear View

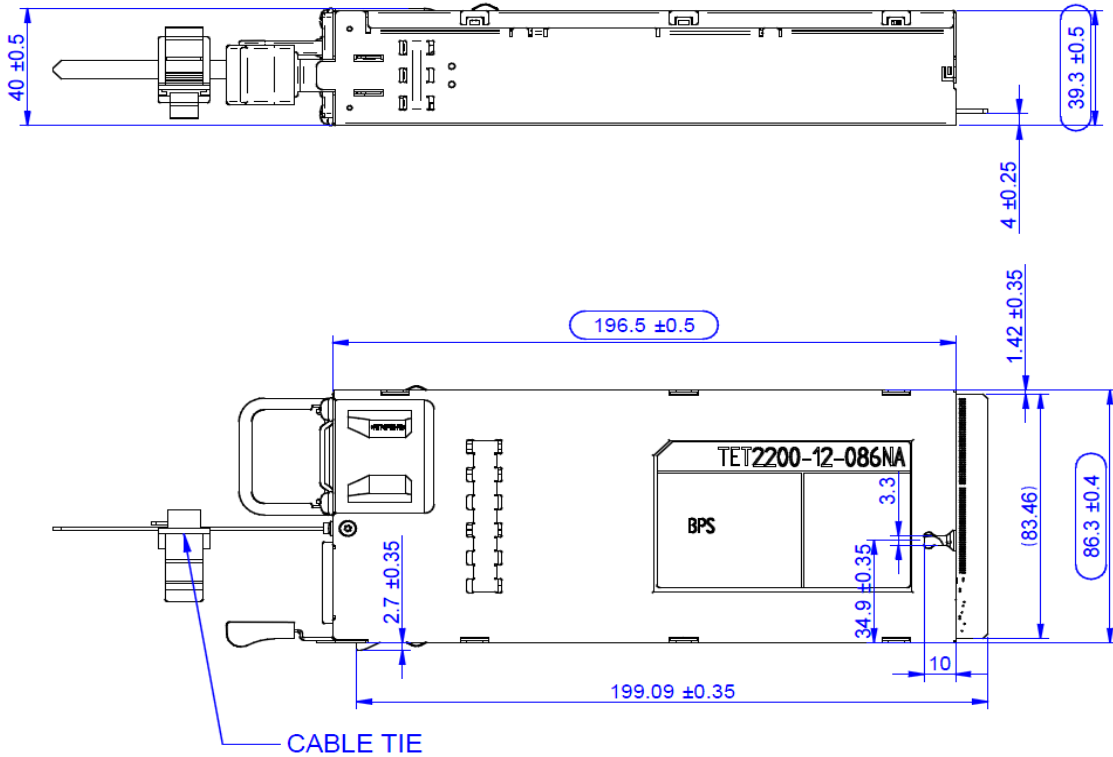


Figure 39. Mechanical Drawing - Side / Top View

NOTE: A 3D step file of the power supply casing is available on request.

9. TEMPERATURE AND FAN CONTROL

10.1 FAN CONTROL

To achieve best cooling results sufficient airflow through the supply must be ensured. Do not block or obstruct the air-flow at the rear of the supply by placing large objects directly at the output connector. The TET2200-12-086NA is provided with a rear to front airflow, which means the air enters through the DC-output of the supply and leaves at the AC-inlet and TET2200-12-086RA is reversed. The fan inside of the supply is controlled by a microprocessor. The rpm of the fan is adjusted to ensure optimal supply cooling and is a function of output power and the inlet temperature.

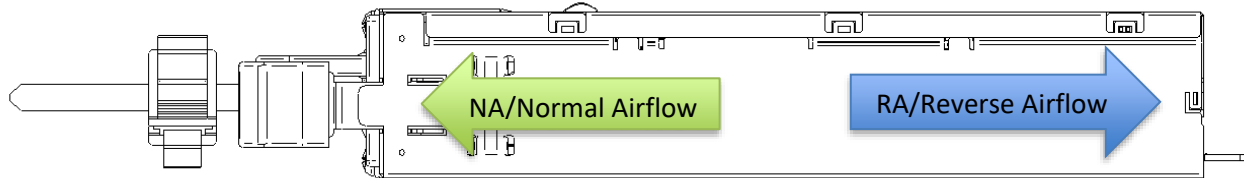


Figure 40. Airflow Direction

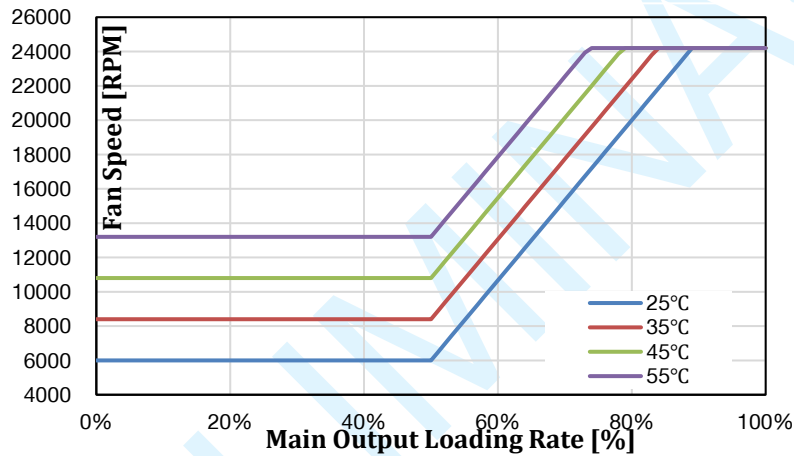


Figure 41. Fan Speed vs. Main Output Load

10.2 TEMPERATURE MONITOR AND OVER TEMPERATURE PROTECTION

The TET2200-12-086 Series provides access via I2C to the measured temperatures of in total 4 sensors within the power supply, see *Table 9*. The microprocessor is monitoring these temperatures and if warning threshold of one of these sensors is reached it will set fan to maximum speed. If temperatures continue to rise above shut down threshold the main output V1 (or VSB if auxiliary converter is affected) will be disabled. At the same time the warning or fault condition is signaled accordingly through LED, PWOK and SMB_ALERT_L.

| TEMPERATURE SENSOR | DESCRIPTION / CONDITION | POWER MANAGEMENT BUS REGISTER | WARNING THRESHOLD | SHUT DOWN THRESHOLD |
|------------------------|---|-------------------------------|--------------------|----------------------|
| Inlet air temperature | Sensor located on inlet | 0x8D | NA:65C RA:60C | NA:70C RA:65C |
| Oring Mosfet | Sensor located close to Oring Mosfet | 0x8E | NA:100C RA:115C | NA:105C RA:120C |
| Outlet air temperature | Sensor located on outlet | 0x8F | NA:85C RA:90C | NA:90C RA:95C |
| PFC&DC-DC heat sink | Sensor located on PFC heatsink and DC-DC heatsink | | | NA: 130C RA: 130C |

Table 9. NA revision Temperature Sensor Location and Thresholds



Asia-Pacific
+86 755 298 85888

Europe, Middle East
+353 61 225 977

North America
+1 408 785 5200

10. ELECTROMAGNETIC COMPATIBILITY

11.1 IMMUNITY

| PARAMETER | DESCRIPTION / CONDITION | CRITERION |
|---------------------------------|--|-------------------------|
| ESD Contact Discharge | IEC / EN 61000-4-2, ± 8 kV, 25+25 discharges per test point (metallic case, LEDs, connector body) | A |
| ESD Air Discharge | IEC / EN 61000-4-2, ± 15 kV, 25+25 discharges per test point (non-metallic user accessible surfaces) | A |
| Radiated Electromagnetics Filed | IEC / EN 61000-4-3, 10 V/m, 1 kHz/80% Amplitude Modulation, 1 μ s Pulse Modulation, 10 kHz...2 GHz | A |
| Burst | IEC / EN 61000-4-4, level 3 AC port ± 2 kV, 1 minute DC port ± 1 kV, 1 minute | A |
| Surge | IEC / EN 61000-4-5 Line to earth: level 3, ± 2 kV Line to line: level 2, ± 1 kV | A |
| RF Conducted Immunity | IEC/EN 61000-4-6, Level 3, 10 Vrms, CW, 0.1 ... 80 MHz | A |
| Voltage Dips and Interruptions | IEC/EN 61000-4-11 1) Vi 230Volts, 70% Load, Dip 100%, Duration 10ms 2) Vi 230Volts, 100% Load, Dip 100%, Duration < 50 ms 3) Vi 230Volts, 100% Load, Dip 100%, Duration > 50 ms | A V1: B; VSB: A B |

Table 10. Immunity

11.2 EMISSION

| PARAMETER | DESCRIPTION / CONDITION | CRITERION |
|--------------------|---|-----------|
| Conducted Emission | EN55022 / CISPR 22: 0.15 ... 30 MHz, QP and AVG | Class A |
| Radiated Emission | EN55022 / CISPR 22: 30 MHz ... 1 GHz, QP | Class A |
| Harmonic Emissions | IEC61000-3-2, Vin = 230 VAC, 50 Hz, 100% Load | Class A |
| AC Flicker | IEC / EN 61000-3-3, $d_{max} < 3.3\%$ | Pass |
| Acoustical Noise | Sound power statistical declaration (ISO 9296, ISO 7779, IS9295) @ 50% load | 50 dBA |

Table 11. Emission

11. SAFETY / APPROVALS

Maximum electric strength testing is performed in the factory according to IEC/EN 60950, and UL 60950. Input-to-output electric strength tests should not be repeated in the field. Bel Power Solutions will not honor any warranty claims resulting from electric strength field tests.

| PARAMETER | DESCRIPTION / CONDITION | MIN | NOM | MAX | UNIT |
|--------------------------|---|------|-----|-----|----------------------|
| Agency Approvals | CAN/CSA-C22.2 No. 62368-1:14 | | | | |
| | UL 62368-1 2nd Ed. | | | | |
| | IEC 60950-1:2005 | | | | |
| | EN 60950-1:2006 | | | | |
| | IEC/EN62368-1:2014 | | | | |
| | BSMI: CNS13438 (95 version), CNS14336-1 (99 version) | | | | Approvals In Process |
| | CQC: GB17625.1-2012, GB4943.1-2011, GB/T9254-2008 (Class A) | | | | |
| Isolation Strength | Input (L/N) to case (PE) | | | | Basic |
| | Input (L/N) to output | | | | Reinforced |
| Creepage / Clearance | Primary (L/N) to protective earth (PE) | 3.0 | | | mm |
| | Primary to secondary | 6.0 | | | |
| Electrical Strength Test | Input to case | 2121 | | | VDC |
| | Input to output | 4242 | | | |

Table 12. Safety/Approvals

12. ENVIRONMENTAL

Power supply shall meet the thermal requirements under the load and environmental condition identified in each table. Even though the table addresses only the exhaust air temperature, all other components in the power supply shall also meet their temperature specifications and lifetime requirements.

The power supply must meet UL enclosure requirements for temperature rise limits. All sides of the power supply with exception to the air exhaust side must be classified as "Handle, knobs, grips, etc. held for short periods of time only".

In case the exit air temperature requirement cannot be met, the power supply must have a warning label for high touch temperature in compliance with IEC/UL 60950-1 and additionally 85°C rated power cords must also be used with this power supply.

| PARAMETER | DESCRIPTION / CONDITION | MIN | NOM | MAX | UNIT |
|---------------------------------|---|-----|-----|------|------|
| T_A Ambient Temperature | V_{min} to V_{max} , I_{nom} , $I_{SB nom}$ at 5000 m | 0 | | +50 | °C |
| | V_{min} to V_{max} , I_{nom} , $I_{SB nom}$ at 2000 m | 0 | | +55 | °C |
| T_{Aext} Extended Temp. Range | Derated output at 2000 m | +50 | | +60 | °C |
| T_S Storage Temperature | Non-operational | -40 | | +70 | °C |
| Altitude | Operational, above Sea Level | - | | 5000 | m |

Table 13. Operation Environmental

13. CONNECTIONS

| PARAMETER | DESCRIPTION / CONDITION | MIN | NOM | MAX | UNIT |
|-------------------------|--|-----|-----|-----|------|
| AC inlet | IEC 60320 C20 | | | | |
| AC cord requirement | Wire size | | 16 | | AWG |
| Output connector | 48 Power + 16 signals Pins PCB card edge | | | | |
| Mating output connector | Manufacturer : FCI Electronics Manufacturer P/N: 10053363-200LF (Right angle without key) BEL P/N: ZES.01359 | | | | |

For the pin assignment of DC connector, please refer to *Figure 42* and *Table 14*.

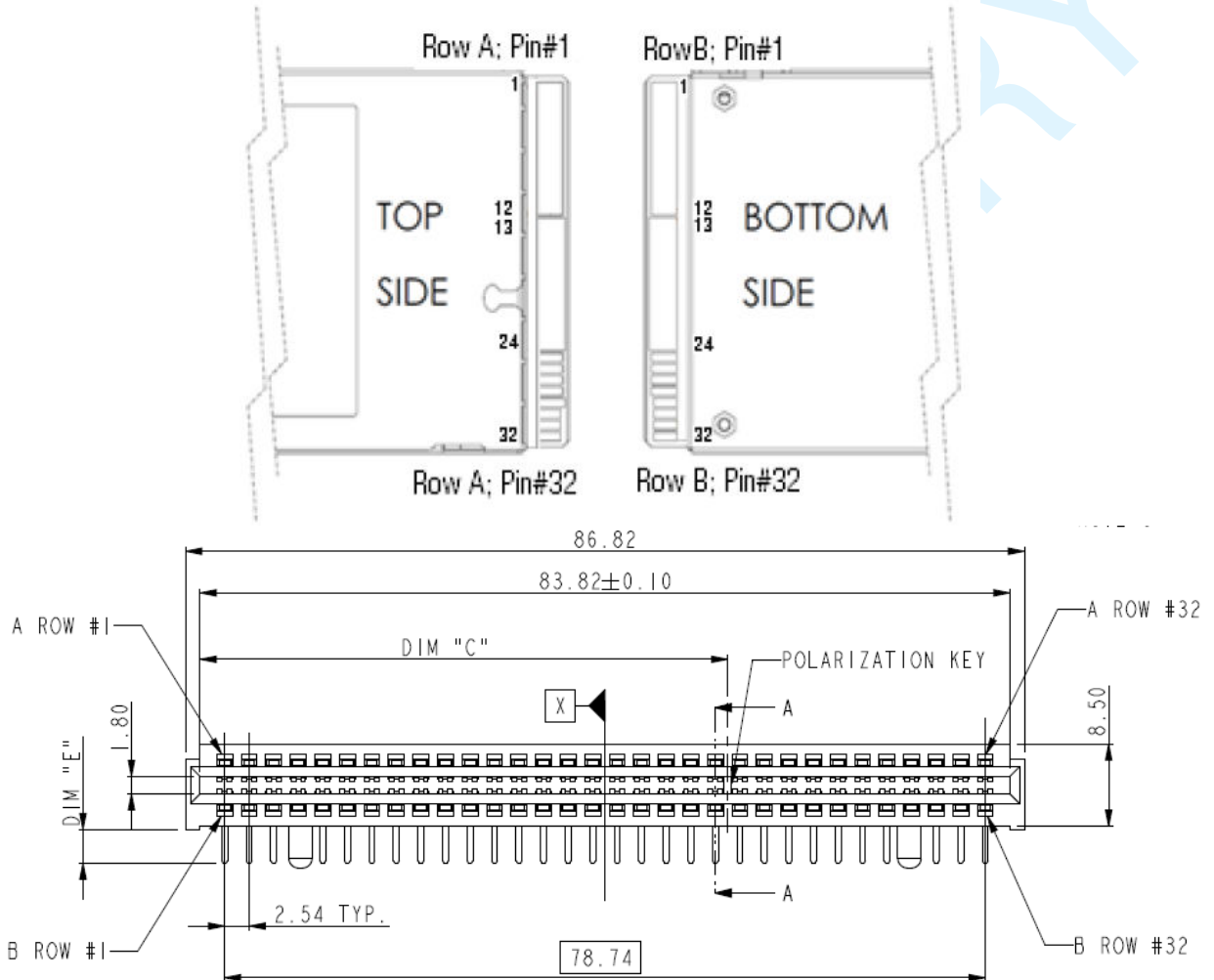


Figure 42. Pin Assignment of DC Connector

| Row A | | | | |
|--------|----------------------------|---------------------------|-----------------|--|
| PIN | NAME | PIN TYPE | Mating Sequence | DESCRIPTION |
| P1-12, | 12V output | 12V Main Output | STD | 12 VDC main output |
| P13-24 | PWR Return | | Long | 12V Main and 12Vsb output return |
| P25 | +12V Remote Sense Input | Input | STD | 12V Output Remote Sense |
| P26 | 12VSTBY | Aux/Standby Power | STD | 12VSTANDBY output |
| P27 | A0 | Input | STD | Power Management Bus address A0 |
| P28 | PWOK | Output | STD | Active high; indicates 12V Main is valid and within operational limits |
| P29 | Signal Return Output | Signal GND | Long | Signal GND; (MFBL) long connection |
| P30 | SCL | Bi-Directional; I/O | Short | I ² C /SMBus/ Power Management Bus Clock Line |
| P31 | PRESENT | Output | Short | Power Supply Present; passive signal to Signal Return |
| P32 | SDA | Bi-Directional; I/O | Short | I ² C /SMBus/ Power Management Bus Data Line |
| Row B | | | | |
| PIN | NAME | PIN TYPE | Mating Sequence | DESCRIPTION |
| P1-12, | 12V Output | 12V Main Output | STD | 12 VDC main output |
| P13-24 | PWR Return | | Long | 12V Main and 12VSB Output return |
| P25 | Smart Redundant Bus Signal | I/O | STD | Smart share for system efficiency performance Common bus to all sharing power modules |
| P26 | Return Sense | Analogue Input | STD | 12V main output Remote Sense Return |
| P27 | ACOK | Output | STD | Indicate AC voltage is present and within operational limits. |
| P28 | 12V Load Share Bus | Bi-Direction Analogue I/O | STD | 12V Main Output Current Share Signal (bus) |
| P29 | PSON | Input | STD | Active low; 12V main output on/off control |
| P30 | PS_KILL | Input | Short | Turns power module on/off, short (MLBF) contact. |
| P31 | No Connection | | Short | No End User Connection |
| P32 | SMB_Alert | Output | Short | Active low; I2C alert signal (interrupt) |

All signal pins are referred to SGND

Table 14. Connector pin assignment

14. REVISION HISTORY

| REVISION | DESCRIPTION OF CHANGES | DATE | ORIGINATOR |
|----------|---|---------------|------------|
| 001 | Initial release | April-11-2019 | Zhiqun Wan |
| 002 | Correct current limitation, update pin assignment | May-08-2019 | Zhiqun Wan |

For more information on these products consult: tech.support@psbel.com

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